AMENDMENTS TO CLAIMS

- Please delete claims 33-35.
- Please amend pending claims 1, 9, and 20, as indicated below. A complete listing of all claims and their status in the application are as follows:

1. (currently amended) A method for fabricating IC's comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask over the intermetal dielectric layer, the bi-layered hard mask comprising a first hard mask layer HM1 overlying a second hard mask layer HM2;

(e) patterning the intermetal dielectric layer and hard mask layers, and CF_4 / N_2 / O_2 based reactive ion etching to form via openings extending through the intermetal dielectric layer and one of the hard mask layers;

(f) forming a layer of via-fill material of bottom anti-reflective coating with photoresist over the intermetal dielectric layer, the via-fill material filling the via openings;

(g) patterning the via-fill material, intermetal dielectric layer and hard mask layers, and etching to form trench openings using a reactive ion etch; and

(h) stripping-off the via-fill material after forming the trench openings, thus forming open trench and open via regions for subsequent conducting metal fill.

2. (original) The method of claim 1, wherein said substrate is semiconductor single crystal silicon or an IC module.

3. (previously presented) The method of claim 1, wherein said conducting material is metal wiring or contacts of Cu, A1Cu alloys, AlCuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

4. (previously presented) The method of claim 1, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide, undoped silicate glass, Fluorine doped Oxide, Carbon-doped Oxide, Organic based low-k dielectric, or porous

low-k dielectric, where the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

5. (previously presented) The method of claim 1, wherein said bi-layered hard mask is comprised of:

first hard mask layer HM1 of undoped silicate glass or SiO_2 film having a thickness in the range from 1000 to 2000 Angstroms; and

second hard mask layer HM2 of silicon carbide or silicon nitride having an etch Selectivity of ~3-5 with respect to said first hard mask layer HM1 and having a thickness of between approximately 300 to 600 Angstroms.

6. (previously presented) The method of claim 1, wherein said photoresist is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

7. (previously presented) The method of claim 1, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching an opening in said via-fill material;

Step 2: CF_4 / CHF_3 / Ar based for HM1. etch;

Step 3: N_2 / O_2 based for etching via-fill material recess;

Step 4: CF_4 / N_2 / O_2 based for etching HM2 and said intermetal dielectric;

Step 5: O_2 based for Ashing; and

Step 6: CHF_3 / N_2 based for bottom etch stop layer etch.

8. (previously presented) The method of claim 1, wherein multilevel structures are fabricating by repeating steps (b) through (h).

9. (currently amended) A method of fabricating an integrated circuit with a dual damascene process using a bi-layer hard mask, the method comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask, two hard mask layers, over the intermetal dielectric layer, the bi-layered hard mask comprising a first hard mask layer HM1 overlying a second hard mask layer HM2;

(e) patterning the intermetal dielectric layer and hard mask layers, and CF_4 / N_2 / O_2 based reactive ion etching to form via openings extending through the intermetal dielectric layer and one of the hard mask layers;

(f) forming a layer of via-fill material of bottom anti-reflective coating with photoresist over the intermetal dielectric layer, the via-fill material filling the via openings;

(g) patterning the via-fill material, intermetal dielectric layer and hard mask layers, and etching to form trench openings using a reactive ion etch;

(h) stripping-off the via-fill material after forming the trench openings, forming open trench and open via regions;

(i) depositing a copper seed layer in the trench openings and via openings;

(j) forming an excess of copper metal over the copper seed layer; and

(k) planarizing the excess copper back, thus forming inlaid copper in the trench and via openings for contact vias and interconnect wiring.

10. (original)The method of claim 9, wherein said substrate is semiconductor single crystal silicon or an IC module.

11. (previously presented) The method of claim 9, wherein said conducting material is metal wiring or contacts of Cu, A1Cu alloys, A1CuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

12. (previously presented) The method of claim 9, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide, undoped silicate glass, Fluorine doped Oxide, Carbon-doped Oxide, Organic based low-k dielectric, or porous low-k dielectric, where the IMD, inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

13. (previously presented) The method of claim 9, wherein said bi-layered hard mask is comprised of:

a first hard mask HM1 layer of undoped silicate glass or SiO_2 having a thickness in the range from 1000 to 2000 Angstroms; and

a second hard mask layer HM2 of silicon carbide or silicon nitride having an etch Selectivity of ~3-5 with respect to said first hard mask layer HM1 and having a thickness of between approximately 300 to 600 Angstroms.

14. (previously presented) The method of claim 9, wherein said photoresist is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

15. (previously presented) The method of claim 9, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching an opening in said via-fill material;

Step 2: CF_4 / CHF_3 / Ar based for HM1. etch;

Step 3: N_2 / O_2 based for etching via-fill material recess;

Step 4: CF_4 / N_2 / O_2 based for etching of said HM2 and said intermetal dielectric;

Step 5: O_2 based for Ashing; and

Step 6: CHF_3 / N_2 based for bottom etch stop layer etch.

16. (original) The method of claim 9, further comprising depositing and defining a copper seed layer, in the via and trench openings, comprised of copper, with thickness maximum of approximately 3,000 Angstroms.

17. (original) The method of claim 9, further comprising depositing a conducting metal fill of electrochemically deposited copper upon a copper seed layer, in the via and trench openings, with thickness maximum of approximately 20,000 Angstroms, forming an excess of copper over the vias and trenches.

18. (original) The method of claim 9, further comprising planarizing an excess of copper over the vias and trenches by chemical mechanical polish, milling, ion milling, and/or etching, forming inlaid dual damascene conducting metal interconnects and contact vias in the vias and trenches.

19. (previously presented) The method of claim 9, wherein multilevel structures are fabricating by repeating steps (b) through (k).

20. (currently amended) A method of fabricating an integrated circuit with a dual damascene process for applications in MOSFET CMOS memory and logic devices, using a bi-layer hard mask, the method comprising the following steps:

(a) providing a substrate with an insulating layer over the substrate;

(b) providing a first level of conducting material defined and embedded in the insulating layer over the substrate;

(c) depositing an intermetal dielectric layer over the insulating layer;

(d) forming a bi-layered hard mask, two hard mask layers, over the intermetal dielectric layer, the bi-layered hard mask comprising a first hard mask layer HM1 overlying a second hard mask layer HM2;

(e) patterning the intermetal dielectric layer and hard mask layers, and CF_4 / N_2 / O_2 based reactive ion etching to form via openings extending through the intermetal dielectric layer and one of the hard mask layers;

(f) forming a layer of via-fill material of bottom anti-reflective coating with photoresist over the intermetal dielectric layer, the via-fill material filling the via openings;

(g) patterning the via-fill material, intermetal dielectric layer and hard mask layers, and etching to form trench openings using a reactive ion etch;

(h) stripping-off the via-fill material after forming the trench openings, forming open trench and open via regions;

(i) depositing a copper seed layer in the trench openings and via openings;

(j) forming an excess of copper metal over the copper seed layer; and

(k) planarizing the excess copper back, thus forming inlaid copper in the trench and via openings for contact vies and interconnect wiring.

21. (original) The method of claim 20, wherein said substrate is semiconductor single crystal silicon or an IC module.

22. (previously presented) The method of claim 20, wherein said conducting material is metal wiring or contacts of Cu, A1Cu alloys, A1CuSi alloys, W, polysilicon, silicide, or P-N junction diffusion regions.

23. (previously presented) The method of claim 20, wherein the insulating layer and intermetal dielectric layer are comprised of: silicon dioxide, silicon oxide, undoped silicate

glass, Fluorine doped Oxide, Carbon-doped Oxide, Organic based low-k dielectric, or porous low-k dielectric, where the IMD inter-metal dielectric, film thickness is in a range approximately from 0.2 to 2 microns.

24. (previously presented) The method of claim 20, wherein said bi-layered hard mask is comprised of:

a first hard mask layer HM1 of undoped silicate glass or SiO_2 having a thickness in the range from 1000 to 2000 Angstroms; and

a second hard mask layer HM2 of silicon carbide or silicon nitride having an etch Selectivity-of ~3-5 with respect to said first hard mask layer HM1 and having a thickness of between approximately 300 to 600 Angstroms.

25. (previously presented) The method of claim 20, wherein said photoresist is comprised of organic material, thickness ranges from thickness from 500 to 3,000 Angstroms, and etched forming trench openings using a reverse tone process.

26. (previously presented) The method of claim 20, wherein the intermetal dielectric layer and hard mask layers are etched to form trench openings by reactive ion etch, RIE, processing scheme for trench etch using the following RIE gas mixtures:

Step 1: CF_4 / Ar based for etching an opening in said via-fill material;

Step 2: CF_4 / CHF_3 / Ar based for HM1 etch;

Step 3: N_2 / O_2 based for etching via-fill material recess;

Step 4: CF_4 / N_2 / O_2 based for etching said HM2 and said intermetal dielectric;

Step 5: O_2 based for Ashing; and

Step 6: CHF_3 / N_2 based for bottom etch stop layer etch.

27. (original) The method of claim 20, further comprising depositing and defining a copper seed layer, in the via and trench openings, comprised of copper, with thickness maximum of approximately 3,000 Angstroms.

28. (original) The method of claim 20, further comprising depositing a conducting metal fill of electrochemically deposited copper upon a copper seed layer, in the via and trench openings, with thickness maximum of approximately 20,000 Angstroms, forming an excess of copper over the vias and trenches.

29. (original) The method of claim 20, further comprising planarizing an excess of copper over the vias and trenches by chemical mechanical polish, milling, ion milling, and/or etching, forming inlaid dual damascene conducting metal interconnects and contact vias in the vias and trenches.

30. (previously presented) The method of claim 20, wherein multilevel structures are fabricating by repeating steps (b) through (k).

31. (canceled)

32. (canceled)

33. (canceled)

34. (canceled)

35. (canceled)